IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: Reflection-Control System and Method
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Technical Field

[0001] The present invention relates to maintaining signal integrity on transmission lines and, in particular, to dampening transmission line reflections.

Background of the Invention

[0002] Transmission line termination refers to strategies or systems used to cancel, mitigate, or dampen signal reflections on transmission lines. Appropriate termination techniques also mitigate other signal integrity problems such as "ringing" oscillations and signal delays. When electronic circuitry employs high-speed components such as fast microprocessors, for example, it is particularly helpful to include proper termination impedance-matching strategies in signal transmission line designs.

[0003] As the speed of digital circuits increases, a number of characteristics related to signal integrity and transmission line behavior deteriorate. It can be expected, for example, that as clock rates rise, crosstalk, the unintended influence of a line's electromagnetic field on other signals, increases. For example, when the clock rate of a system doubles, crosstalk tends to double. Further, as signal speeds increase, electromagnetic noise increases, thus affecting signal integrity. Adding an increased number of power and ground connections and more bypass capacitors to shunt electromagnetic noise may help mitigate these effects. At some point, however, new strategies to minimize transmission line reflections and crosstalk will be needed to preserve signal integrity.

[0004] At today's speeds, even the passive elements of a high-speed design, features such as the wires and printed circuit board (PCB) traces, for example, as well as chip packages, can contribute significantly to overall signal delay and exacerbate timing and logic errors. The secular move toward ever-increasing speeds without commensurate improvements in transmission line signal management and termination will make signal integrity preservation an escalating issue in high speed electronics.

[0005] Driver characteristics may be modified to improve signal integrity. Lower output impedance drivers tend to drive heavily loaded signals more quickly. Drivers with controlled variation in output impedance from cycle to cycle also tend to improve transmission line impedance matching thus inhibiting reflection behavior. Lower transmission line impedances and lower driver output impedances typically result, however, in higher power consumption as lower impedances dissipate more power.

[0006] Signal integrity management strategies typically include appropriate termination structures devised to inhibit signal reflections that arise on the transmission line. Unfortunately, termination structures occupy space and

dissipate power. Designers in the art, therefore, sometimes avoid adding physical termination structures to board designs.

[0007] Two principle techniques are employed in termination structures: source (series) termination and load (parallel) termination. Source or series termination places an impedance (many times a simple resistor) between the signal driver and the transmission line. Load or parallel termination places an impedance parallel with the receiver or load at terminal point of the transmission line. Sometimes the two methods are combined.

[0008] Because source impedance is typically more predictable than load impedance, a series termination impedance typically better matches the impedance of a transmission line than does the impedance of a parallel termination scheme. Further, because a series termination, unlike a parallel termination, does not typically consume appreciable power after the line is driven HIGH, a series termination often consumes less power than does a parallel termination. Series terminations typically present, however, a relatively high series impedance that can impede signal integrity by increasing the transmission line RC characteristic.

[0009] The basic termination schemes are often seen in a variety of modified forms. One technique adjusts, for example, an on-chip variable parallel termination to match a reference resistor. The on-chip termination is typically a network of parallel resistors controlled by series switches and a feedback circuit. This scheme uses little PCB space but, like many parallel termination schemes, can dissipate power even after the transmission line has been driven HIGH. One example of such a technique is purportedly depicted in United States Patent 6,605,958 to Bergman, et al. It also can be difficult to terminate a complex topology like a DRAM address net.

[00010] Other techniques have been developed for matching transmission line impedance. One such scheme employs an adaptive transmission line termination

including a linearly-variable resistor connected either in series with the sending end of a transmission line or, in parallel with the receiving end of the line. A feedback circuit varies the resistance to constantly match line impedance. This scheme attempts to mitigate cycle-to-cycle variance in transmission line and driver output impedances. When in series mode, this termination does not switch to a lower impedance when the line is driven HIGH and, consequently, does not mitigate the RC effect of the higher impedance that is often characteristic of series termination strategies. An example of this scheme is purportedly depicted in United States Patent 5,422,608 to Levesque.

[00011] United States Patent 6,265,893 to Bates depicts a system in which drivers are coupled to different points on a transmission line. The drivers each include a transistor in series with a resistance that matches the transmission line impedance. The transistor at one driver is ON to provide a load end parallel termination whenever another driver might be active. This system and many others like it, allow multiple devices to drive signals on the same transmission line, but they still exhibit problems inherent to parallel termination schemes such as higher power consumption and imprecise impedance matching, for example.

[00012] In any of the known termination schemes, when no load termination is used, the input impedance of the receiver is present at the load end of the transmission line. This impedance is typically a complex value with capacitive and resistive components. Because the typical receiver input resistance is higher than the transmission line impedance, the mismatch induces a reflection. This reflection wave or impulse can travel with an uncontrolled characteristic on the transmission line and impede or, in some cases, prevent accurate signal reception.

[00013] What is needed, therefore, is a technique and system for terminating a transmission line to reduce reflections, improve signal integrity, and drive the line

HIGH quickly while presenting lower impedances and consuming minimal PCB space.

Summary of the Invention

[00014] A transmission line is terminated with a series termination circuit that changes impedance in relation to the timing of applied signals. The impedance of the series termination circuit changes from a short circuit (or near short) to a matched impedance after substantial energy of an applied signal passes through the series termination circuit to the transmission line but before an initial signal reflection returns from a load end of the transmission line.

[00015] In a preferred embodiment of the invention, the system includes a series termination that substantially matches the transmission line impedance and a switch connected in parallel to the series termination. The switch closes before the transition of an applied signal. After the signal is applied through the closed switch but before an initial reflection arrives back at the driver site of the transmission line, the switch opens, placing the series termination between the driver and the transmission line.

Brief Description of the Drawings

[00016] FIG. 1 depicts a prior art circuit illustrating series and parallel termination schemes.

[00017] FIG. 2 is a symbolic depiction of a preferred embodiment of the invention.

[00018] FIG. 3 is an alternative symbolic depiction of an alternative embodiment of the invention.

[00019] FIG. 4 depicts a further alternative embodiment of the invention.

[00020] FIG. 5 depicts another embodiment of the invention.

[00021] FIG. 6 is a timing diagram illustrating signals and events related to one embodiment of the invention.

[00022] FIG. 7 is a flow chart of a procedure for configuring certain embodiments of the present invention.

[00023] FIG. 8 is graph of a rising load voltage according to one embodiment of the present invention.

Detailed Description of Preferred Embodiment

[00024] FIG. 1 depicts a prior art circuit illustrating examples of series and parallel termination schemes. As shown in FIG. 1, basic driver 12 receives a signal "S" to be transmitted. Basic driver 12 typically transmits signal "S" from its output by applying digital HIGH and LOW signals, which typically have rising edges and falling edges during transitions between HIGH and LOW values. Basic driver 12 may be any of a variety of drivers including, for example, a Gunning Transistor Logic (GTL) style driver, a tri-state driver, or a complementary pair driver. These are just examples and those of skill in the art will recognize that the principles described here are applicable to a wide variety of driving circuits and conductive elements and media that exhibit transmission line behavior in the conveyance of energy.

[00025] Basic driver 12 is connected to a first terminal 13 of the series termination 14. Series termination 14 is also known as a "source termination" and may be referred to as either a source or series termination.

[00026] Although illustrated for ease of depiction as a resistance element, those of skill will recognize that in many circuits, series termination 14 is a complex

impedance, that is, it exhibits capacitance and inductance. Series termination 14 may also be an active component or a combination of active components, such as, for example, a transistor with a controlled input voltage to present a characteristic impedance useful in source termination. Series termination 14 is preferably devised to present an impedance that matches the impedance of transmission line 16 to cancel or dampen signal reflections that may arise in system 10.

[00027] The second terminal 15 of series termination 14 is connected to the proximal end "P" of transmission line 16. Transmission line 16 is devised to convey electrical signals from basic driver 12 to one or more receivers. Transmission line 16 is typically a PCB trace, but may take many forms including, for example, coaxial cable, wires, wire pairs, ribbon cables, back-plane PCB traces and connectors, optical fibers, waveguides or dielectric slabs, or combinations of these and other signal lines known in the art. As is well-known, other circuit elements may exhibit electro-magnetic field and propagation effects (such as mutual inductance, capacitance, and reflections) of a theoretical transmission line and although the invention may be used profitably with transmission lines 16 that exhibit classic transmission line behavior, the use of the invention is not limited to those systems where transmission line 16 meets that definition but may be used to advantage in the wide variety of types, lengths, and sizes of media used to convey energy. Further, other elements, such as, for example, on-die signal paths, pins of packaged integrated circuits, connectors, stacking connectors, and other elements known in the art may be considered as being part of transmission line 16 exemplified in the Figures herein. Transmission line 16 is shown as being broken with separating lines to indicate that it may have significant length. Transmission line 16 may further include several "ends" that branch out and/or terminate at several different locales or sub-circuits. Transmission line 16 is depicted with only

one distal end "D", but as those of skill will recognize, it may have many distal ends.

[00028] Distal end "D" of transmission line 16 is connected to the receiver load 18, which is shown as being connected in parallel with a parallel termination 17. The depicted parallel termination 17 may appear on a transmission line with or without an accompanying series termination 14. It is well known to those of skill in the art that termination 17 may include a complex impedance or active elements such as transistors, for example. In any case, termination 17 is preferably devised to match the impedance of receiver load 18 to the impedance of transmission line 16.

[00029] Receiver load 18 is represented in FIG. 1 by a capacitive circuit to depict the capacitive characteristics which are typically quite relevant to signal integrity. Receiver load 18 may also, in this specification, be referred to as "receiver 18" or "load 18", however, those of skill in the art will recognize that the depiction of load 18 as a capacitive feature is a heuristic simplification of more complex phenomena and structure. Receiver 18 is the reception point for signals conveyed by transmission line 16 and, in practice, receiver 18 typically passes received signals to other circuits "downstream" from receiver 18. Such other circuits are not shown in FIG. 1 to simplify the illustration. Most receivers have a high input resistance which is not represented as a separate circuit element because high input resistances do not typically introduce large or significant errors into the operation of the circuit. However, the capacitance of load 18 affects the resistive/capacitive time constant of the circuit and is, therefore, symbolically depicted.

[00030] FIG. 2 illustrates in system 20 a preferred embodiment of the present invention devised to inhibit deleterious reflections. System 20 includes reflection control driver 30, transmission line 16 and load 18. Those of skill will recognize that transmission line 16 and load 18 are idealized representations and may include

complex topologies and behavioral attributes arising from multiple taps and branches, in the case of transmission line 16, for example, and, complex inductive behavior in the case of load 18, for example.

[00031] Reflection control driver 30 includes basic driver 12, switch 31, and series termination 14. Basic driver 12 can be any type of driver known in the art. Preferably, basic driver 12 has an output impedance of less than 2 ohms. As those of skill in the art will understand, basic driver 12 is presented with signal S to be conveyed on transmission line 16. Basic driver 12 conditions signal S for conveyance on transmission line 16 and presents a conditioned signal at output 32. The conditioned signals are typically binary signals that have HIGH and LOW voltages representing binary 1's and 0's. These signals must pass through switch 31 and/or termination 14 to reach transmission line 16 and receiver 18. Preferably, in an integrated semiconductor implementation of the depicted embodiment, switch 31 and termination 14 are located on-die, near basic driver 12.

[00032] Termination 14 is connected in series between driver output 32 and the proximal end P of transmission line 16. Termination 14 may be any type of termination known in the art, including, but not limited to, those discussed with regard to FIG. 1. Switch 31 is connected in parallel to termination 14 such that when switch 31 is closed, a signal can propagate from driver output 32 through switch 31 to transmission line 16. Switch 31 has a control terminal 34 which receives control signals and causes switch 31 to close or open in response thereto. Preferably, control terminal 34 is a binary type input terminal. In this preferred embodiment, control terminal 34 is connected to driver output 32, although those of skill will recognize that control terminal 34 may be controlled by any of a variety of well known timing and control schemes including passive and active techniques.

[00033] In a preferred embodiment, control terminal 34 operates to open switch 31 some predictable delay period after basic driver 12 applies a rising-edged signal to control terminal 34. Consequently, the rising-edged signal passes through closed switch 31 to proximal end P of transmission line 16. Consequently, substantially all of the impulse of the rising-edged signal propagates through closed switch 31 rather than termination 14. When the rising-edged signal travels through transmission line 16 and reaches receiver 18, a reflection is precipitated by the impedance mis-match between receiver 18 and transmission line 16. When the reflection returns to proximal end P of transmission line 16, the delay period between the application of the rising-edged control signal upon control terminal 34 and the consequent opening of switch 31 has passed. Consequently, with switch 31 opened, the reflection is diverted to pass through termination 14. Termination 14, chosen to match the impedance of reflection control driver 30 to the impedance of transmission line 16 dampens the return reflection.

[00034] Although a rising-edged signal has been introduced, those of skill in the art will realize after appreciating this specification that a variety of signaling schemes having a variety of signal transitions producing reflection wave-fronts can be effectively managed using the invention. With a transmitting scheme that uses negative voltage levels or more than two voltage levels, for example, the invention may be used to advantage at each signal transition which produces, in that particular signaling scheme, a reflection. The desired delay time of switch 31 and the related timing exhibited by the signal reflection on transmission line 16 will be further described with reference to FIG. 6.

[00035] Switch 31 is preferably a high-speed FET switch, but may be any switch fast enough to open and close within the needed timing parameters, a few examples of which are described with reference to FIG. 6. For example, switch 31 may be implemented with a single transistor or a combination of transistors or

other electronic switches known in the art. The delay time of switch 31 may be managed with several possible sources. For example, switch 31 may be chosen so that its inherent switching time matches the desired delay. Other strategies may use a delay element 35 placed to delay the input to control terminal 34 as shown in FIG. 2 as another alternative in delay timing management. If such a delay element 35 is used, it is chosen, preferably, to add to the switching delay of switch 31 to produce the desired delay. Delay element 35 may be implemented by connecting an external element, such as a capacitor, resistor, or length of PCB trace.

[00036] Switch 31 maybe closed, however, any time between dampening of a signal reflection and application of the next transitioning-edged signal from basic driver 12. In preferred applications, switch 31 is closed upon application of a rising-edged signal at control terminal 34 and opens a related delay time later.

[00037] FIG. 3 depicts an alternative embodiment of the present invention. Control terminal 34 is connected to the driver input 40 of basic driver 12 rather than to the output. The embodiment of FIG. 3 may be used when switch 31 is too slow to close in time to dampen the signal reflection. Such an embodiment can deliver a control signal to switch 31 faster than embodiments such as that shown in FIG. 2 because delay in the driver is eliminated. Again, a time delay element may be added to switch 31 if switch 31 closes before the applied rising-edged signal passes through switch 31.

[00038] FIG. 4 depicts another embodiment of the present invention devised to modify and improve alternative series termination schemes. As shown, a series termination is devised with an active termination 50 which, in the depicted embodiment, is a variable resistance. The variable resistance adjusts to impedance changes in transmission line 16 or basic driver 12. There are many ways known in the art to make a variable resistance, and the embodiment depicted here is merely one example that may be employed to advantage in the present invention. Active

termination 50 is connected in parallel with switch 31. The control terminal of switch 31 may be operated as discussed with reference to earlier FIG. 2 or FIG. 3.

[00039] Active termination 50 includes a field effect transistor (FET) 52 connected between the output of basic driver 12 and the proximal end P of transmission line 16. The source terminal of FET 52 is connected through diode 54 to one input of amplifier 56. The other input of amplifier 56 is connected to a reference voltage, VREF, which is typically half of VDD (the voltage representing a high digital signal). The output of amplifier 56 is connected as a feedback to the gate of FET 52. The feedback adjusts the drain-to-source resistance of FET 52 to match the basic driver 12 output impedance to the impedance of transmission line 16; thus keeping the voltage on proximal end P of transmission line 16 close to VREF when switch 31 is open.

[00040] FIG. 5 depicts another alternative embodiment of the present invention. An adjusting termination 60 is shown connected between basic driver 12 and transmission line 16. Adjusting termination 60 has a control terminal 62. In response to input signals, control terminal 62 causes adjusting termination 60 to change from a zero or near zero impedance to an impedance that matches or is close to that of transmission line 16. Those skilled in the art will recognize that many variable resistance circuits may be employed as depicted in the disclosed embodiment. In this embodiment, control terminal 62 is connected to the output of basic driver 12. However, control terminal 62 could be connected to the input of basic driver 12. Adjusting termination 60 exhibits a time delay between the application of an appropriate signal to control terminal 62 and the change to a matching impedance. The time delay is preferably no greater than twice the propagation delay of the transmission line.

[00041] FIG. 6 is a timing diagram depicting the propagation of signal voltages on the circuit of FIG. 2 and selected other embodiments of the present invention.

Waveform 6A represents the voltage appearing between basic driver 12 and series termination 14. Waveform 6B represents the voltage appearing at receiver load 18. Waveform 6C represents the current through series termination 14.

[00042] All of the waveforms are on the same timescale, with time on the horizontal axis. Time T = 0 is the time that basic driver 12 starts to apply a signal. Time "T_D" represents the propagation delay of transmission line 16. That is, the time it takes for a voltage signal to propagate the length of transmission line 16. Time $2T_D$ is the time it takes for a signal to propagate along transmission line 16 added to the time it takes for a reflection to propagate back from the load to reach the driver.

[00043] With reference to waveform 6A, at time T = 0, basic driver 12 applies the rising-edged signal. Time T_{RISE} is the rise time of the rising-edged signal. Rise times for different drivers vary greatly, but some fast drivers might have rise times of 0.05nS to 0.4nS or lower. The applied rising-edged signal propagates along transmission line 16 until it reaches distal end D. The voltage at D is shown in waveform 6B. This waveform shows a rise time T_{LOAD} that is greater than T_{RISE} because transmission line 16 and load 18 absorb energy and disperse the signal. The magnitude of waveform 6B is typically larger than that of 6A because load 18 precipitates an additive reflection that travels back toward control basic driver 30.

[00044] Waveform 6C represents the current through series termination 14. No current flows through termination 14 until time T_S, when switch 31 opens. Until switch 31 opens, all or most of the current flows through switch 31 instead of series termination 14. When switch 31 opens, all or most of the current flows through termination 14.

[00045] The reflection from load 18 causes a spike of current shown on waveform 6C shown at time $2T_D$ and a spike of voltage shown on waveform 6A at time $2T_D$. After the spike shown on waveform 6C, the current through series termination 14

typically drops to near zero amps because load 18 typically has a high input impedance and draws minimal current.

[00046] Waveform 6C is marked with arrows "T_S Range" indicating a range of exemplar times where T_S may be found, i.e., the time when switch 31 opens. Switch 31 preferably opens after time T_{RISE} and before time $2T_D$. However, the switch could open before the rise time is complete if a substantial amount of the energy needed to drive the loaded transmission line HIGH were already applied to the transmission line. Time T_S is preferably somewhere near one-half of the total of $T_D + T_{LOAD}$. Further, time T_S may be chosen in accordance with one embodiment of the invention with equation 1.

[00047] (1) $T_S = \frac{\Pi}{e}$ SquareRoot(((RC)^2 + T_{RISE} ^2)/2),

[00048] where RC is the resistive-capacitive time constant of the entire transmission line circuit, including load 18. RC is calculated as an equivalent RC with switch 31 closed. This equation may yield favorable results for practicing embodiments of the invention even when R, C, and T_{RISE} vary greatly.

[00049] FIG. 7 is a flow chart of a procedure for configuring certain embodiments of the present invention. This procedure may yield favorable results for practicing the invention for a point to point or star transmission line topology driving a heavy load.

[00050] Step 71 determines the basic driver 12 (FIGS. 2-5) rise time T_{RISE} in a "no load" condition. Step 72 determines the total load capacitance C_{LOAD}. One or more receivers connected to transmission line 14 in a point-to-point or star configuration may be added to calculate C_{LOAD}, excluding the transmission line 14 capacitance. Step 73 determines the expected transmission line propagation time, T_{TRAN}. Desired part placement and signal propagation delay per unit length of transmission line largely determine T_{TRAN}.

[00051] Step 74 determines the desired rise time at the load, T_{LOAD}. Certain embodiments of the invention may yield more favorable results when T_{LOAD} is less than the round trip delay time 2* T_{TRAN} of transmission line 14. Step 75 sets the impedance Z of the transmission line based on C_{LOAD} and T_{LOAD}. Impedance Z may be determined in accordance with equation 2.

[00052] (2) $Z=sqrt(2)* T_{LOAD} / C_{LOAD}$

[00053] Equation 2 may be modified to include a correction factor devised to adjust for unloaded rise time T_{RISE}. For operating environments with high load capacitances C_{LOAD} and short values of T_{LOAD}, equation 2 may result in values of impedance Z that are low compared to the lowest values achievable with a particular transmission line or trace technology. Two or more relatively high impedance transmission lines or traces may be employed in parallel to achieve these low impedance Z values. Alternatively, load capacitance C_{LOAD} could be reduced or a longer rise time T_{LOAD} could be chosen by working backwards from the lowest practical impedance Z in a particular operating environment to determine the charge needed on C_{LOAD}.

[00054] With continued reference to FIG. 7, step 76 determines the switching time T_S. Switching time T_S, described with regard to above-referenced FIG. 6, is the time at which series termination 14 impedance changes to match the transmission line impedance. T_S may, in this alternative embodiment of the invention, be approximately determined in accordance with equation 3.

[00055] (3) $T_S =Z* C_{LOAD} /sqrt(2)$

[00056] Switching time T_S may be implemented in a variety of ways. One implementation method is to calculate the T_S required by the application, as described with regard to Step 76, then arrange components such as a capacitor, a resistor, and/or PCB traces with specified lengths to achieve a time delay. Another implementation may use a calibration scheme on a dedicated dummy net to

monitor the current out of the driver. A driver with an optimal T_S value will typically exhibit a zero mA current after the reflection has arrived at the load and the energy in the reflection wavefront has dissipated. Typically, any non-zero current after the reflection has dissipated may be amplified and used as a feedback signal to calibrate T_S.

[00057] FIG. 8 is graph of a rising load voltage wavefrom 8A according to one embodiment of the present invention, configured according to the procedure described with regard to FIG. 7, compared with a conventional series termination driver waveform 8B. The invention may be practiced with advantage to drive a heavy capacitive load through a transmission line with a linear voltage ramp at the load as shown in waveform 8A, until the load substantially reaches the desired voltage rail Vddq, and then an abrupt slow-down in the voltage rise as shown at point 82 on waveform 8A. The change of series termination impedance at time T_S typically causes the current from the driver to be halved. This halving, after a T_{TRAN} delay of 1nS in this exemplar, typically causes the load voltage curve to abruptly flatten, producing a "sharp voltage corner" at the load with minimal overshoot or undershoot, as shown at point 82. In a preferred embodiment, the driver impedance is close to zero ohms. If T_{TRAN} is short relative to the sum of loaded rise time T_{LOAD} and unloaded rise time T_{RISE}, the load slew rate curve may have noticeable change as one or more reflections travel on the un-terminated transmission line before time T_S. In such a case, time T_S may be set to be less than $2^* T_{TRAN}$, and a constant-current driver may be used to advantage to drive energy to finish charging load capacitance through series termination 14.

[00058] Those of skill in the art will realize, after appreciating this specification, that the improved slew rate and voltage margin characteristics described with regard to FIG. 8 may be employed to advantage by lowering the range of HIGH and LOW voltage signals from the typical full voltage range of zero volts to Vddq.

This may be achieved by, for example, driving the load between Vddq*1/4 as a LOW signal and Vddq*3/4 as a HIGH signal. In this exemplar, the driver may achieve a transition to HIGH by signaling at Vddq, and then at time T_S signaling at Vddq*3/4 with series termination 14 in place. Time T_S, in this exemplar embodiment, would be determined according to the procedure described with regard to above-referenced FIG. 7, using, however, a desired rise time at the load in Step 74 adjusted to account for the shorter rise time and smaller load charging energy needed to reach Vddq*3/4. Further, in this exemplar, the driver may achieve a transition to LOW by signaling at ground, and then at time T_S switching to signal at Vddq*1/4 with series termination 14 in place. This exemplar embodiment of the invention may be practiced to advantage to lower transition time between signal levels and reduce power consumption. Further, as those of skill in the art will realize after appreciating this specification, the invention may be employed to advantage in a signaling scheme with multiple signal levels to improve the voltage margin and slew rate of signal transitions.

[00059] Although the present invention has been described in detail, it will be apparent to those skilled in the art that the invention may be embodied in a variety of specific forms and that various changes, substitutions and alterations can be made without departing from the spirit and scope of the invention. The described embodiments are only illustrative and not restrictive and the scope of the invention is, therefore, indicated by the following claims.